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119TH CONGRESS
2D SESSION

S. 4810

To establish a grant program for education related to semiconductor manufacturing and related industries.

IN THE SENATE OF THE UNITED STATES

JUNE 17, 2026

Mr. KELLY (for himself and Mr. BUDD) introduced the following bill; which was read twice and referred to the Committee on Commerce, Science, and Transportation

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A BILL

To establish a grant program for education related to semiconductor manufacturing and related industries.

Be it enacted by the Senate and House of Representatives of the United States of America in Congress assembled,

SECTION 1. SHORT TITLE.

This Act may be cited as the ''CHIPS Training in America Act of 2026''.

SEC. 2. AUTHORIZATION FOR THE CREATING HELPFUL INCENTIVES TO PRODUCE SEMICONDUCTORS (CHIPS) FOR AMERICA WORKFORCE AND EDUCATION FUND.

Section 102(d) of Public Law 117–167 (commonly known as the ''CHIPS and Science Act of 2022'') is amended in paragraph (1) by inserting '', including establishment and maintenance of a single publicly accessible online clearinghouse of microelectronics education and workforce development information'' before the period at the end of the paragraph.

SEC. 3. AUTHORIZATION OF NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER ACTIVITIES.

Section 9906(c)(2) of the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021 (15 U.S.C. 4656(c)(2)) is amended in subparagraph (C)—

(1) in clause (i), by striking ''and'' after the semicolon;

(2) in clause (ii), by striking the period at the end and inserting ''; and''; and

(3) by adding at the end the following:

''(iii) the development of competency-based degree, credentialing, and certificate frameworks to increase standardization

within semiconductor and microelectronics workforce development programs.''.

SEC. 4. NATIONAL STRATEGY ON MICROELECTRONICS WORKFORCE.

Section 9906(a) of the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021 (15 U.S.C. 4656(a)) is amended—

(1) in paragraph (2)—

(A) by redesignating subparagraph (I) as subparagraph (J); and

(B) by inserting after subparagraph (H) the following:

''(I) For purposes of the duties described in subparagraph (D) of paragraph (3) only, the Secretary of Labor, the Secretary of Education, and the Secretary of Veterans Affairs.''.

(2) in paragraph (3), by inserting after subparagraph (C) the following:

''(D) NATIONAL STRATEGY ON MICROELECTRONICS WORKFORCE.—

''(i) IN GENERAL.—

''(I) NATIONAL STRATEGY ON MICROELECTRONICS WORKFORCE DEVELOPMENT.—Not later than 1 year after the date of enactment of the

CHIPS Training in America Act of 2026, in consultation with appropriate stakeholders in the microelectronics industry, relevant researchers or experts at institutions of higher education, economic development organizations, and other apposite stakeholders, the Subcommittee shall develop a 5-year national strategy on microelectronics workforce development.

''(II) ADDITIONAL SUBCOMMITTEE MEMBERS.—For the purposes of this subparagraph only such Subcommittee shall also include the Secretary of Labor, the Secretary of Education, and the Secretary of Veterans Affairs.

''(ii) ELEMENTS.—The strategy developed under this subparagraph shall—

''(I) specify and prioritize annual and long-term objectives, including the role of each agency in supporting programs and activities designed to meet the objectives, to ensure a ro-

bust, skilled domestic microelectronics workforce;

''(II) specify the common metrics that will be used to assess progress toward achieving the objectives;

''(III) describe the roles of and means of coordination with elementary and secondary, and postsecondary, education systems in achieving the objectives;

''(IV) describe how Federal funding will be used to support the strategy's microelectronics workforce initiatives;

''(V) describe the approaches to be taken by each participating agency to assess the effectiveness of the agency's microelectronics workforce programs and activities;

''(VI) describe how objectives outlined in the strategic plan will align with investments made using funds from divisions A and B of Public Law 117–167 (commonly known as

the 'CHIPS and Science Act of 2022');

''(VII) describe how objectives outlined in the strategic plan will align with the objectives of the 5-year STEM education strategic plan required under section 101 of the America COMPETES Reauthorization Act of 2010 (42 U.S.C. 6621); and

''(VIII) describe how objectives outlined in the strategic plan will align with the objectives of the national strategy on microelectronics research, as required under subparagraph (A), as applicable.

''(iii) FOSTERING COORDINATION OF WORKFORCE PROGRAMS.—The Subcommittee shall coordinate programs and activities of Federal agencies relating to microelectronics workforce development, and ensure such programs and activities are consistent with the strategy required under this subparagraph.

''(iv) REPORTING AND UPDATES.—Not less frequently than once every 5 years, the Subcommittee shall—

''(I) update the strategy under this subparagraph;

''(II) submit the revised strategy to the appropriate committees of Congress; and

''(III) make such strategy publicly available through the online clearinghouse authorized in section 102(d) of Public Law 117–167.''.

SEC. 5. GRANT PROGRAM FOR EDUCATION RELATED TO SEMICONDUCTOR MANUFACTURING AND RELATED INDUSTRIES.

Division H of title XCIX of the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021 (15 U.S.C. 4651 et seq.) is amended by inserting after section 9906 the following:

''SEC. 9906A. WORKFORCE DEVELOPMENT ACTIVITIES.

''(a) DEFINITIONS.—In this section:

''(1) ELIGIBLE INSTITUTION.—The term 'eligible institution' means—

''(A) an institution of higher education, as defined in section 101 of the Higher Education

Act of 1965 (20 U.S.C. 1001), at which the highest degree predominantly awarded to students is not a baccalaureate degree or higher degree;

''(B) a postsecondary vocational institution, as defined in section 102(c) of the Higher Education Act of 1965 (20 U.S.C. 1002(c)); and

''(C) an area career and technical education school, as defined in subparagraphs (A) or (B) of section 3(3) of the Carl D. Perkins Career and Technical Education Act of 2006 (20 U.S.C. 2302(3)).

''(2) ELIGIBLE PARTNERSHIP.—The term 'eligible partnership' means a partnership that—

''(A) includes—

''(i) an eligible institution;

''(ii) a covered entity; and

''(iii) a State, Indian Tribe, or political subdivision thereof; and

''(B) may include other entities.

''(3) NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER.—The term 'National Semiconductor Technology Center' means the entity established under section 9906(c).

''(b) GRANTS AUTHORIZED.—The National Semiconductor Technology Center shall make awards, on a competitive basis, to eligible partnerships to establish or expand workforce development and academic programs offered by an eligible institution (which may include short-term programs or non-credit programs offered by that eligible institution), related to semiconductor manufacturing and related equipment, materials, advanced packaging, microelectronics, computer science, engineering, and related industries.

''(c) APPLICATION.—An eligible partnership desiring a grant under this section shall submit an application to the National Semiconductor Technology Center at such time, in such manner, and containing such information as the National Semiconductor Technology Center may require. The application shall require—

''(1) a description of the eligible partnership;

''(2) a description of the workforce needs that will be addressed through the activities funded by the grant;

''(3) a description of the eligible partnership's strategy to sustain such activities after the grant period;

''(4) a description of how the eligible partnership will recruit and retain individuals with barriers

to employment (as defined in section 3 of the Workforce Innovation and Opportunity Act definition (29 U.S.C. 3102)) in programs that receive grant funding; and

''(5) a description of how programs supported by grants under this subsection align with the workforce pathways and credential frameworks established by the National Semiconductor Technology Center or the National Science Foundation.

''(d) SELECTION.—In selecting eligible partnerships to receive a grant under this section, the National Semiconductor Technology Center shall give priority to eligible partnerships located in areas with growing microelectronics ecosystems, as determined by the National Semiconductor Technology Center, that serve or intend to serve as members of broader sectoral partnerships and coordinate with State and local workforce development boards (as established under sections 101 and 107 of the Workforce Innovation and Opportunity Act (29 U.S.C. 3111; 29 U.S.C. 3122)), respectively.

''(e) AMOUNT; DURATION.—

''(1) AMOUNT.—A grant awarded under this section shall be for an amount equal to or less than $7,000,000.

''(2) DURATION.—A grant awarded under this section shall be for a period not to exceed 5 years.

''(f) FEDERAL COST SHARE.—

''(1) MAXIMUM FEDERAL SHARE.—The Federal share of the costs of a grant under this section shall not exceed 50 percent of such costs.

''(2) REQUIRED WORKER AND COMMUNITY INVESTMENTS.—Non-Federal costs contributed by a covered entity under this section shall be considered as part of an eligible entity's commitments to worker and community investments as required under section 9902(a)(2)(B)(ii)(II).

''(g) REPORT.—

''(1) REPORT TO THE NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER.—Each eligible partnership receiving a grant under this section shall prepare and submit an annual report to the National Semiconductor Technology Center that contains information about each of the following with respect to individuals participating in a program funded by a grant under this section:

''(A) The total number of participants, disaggregated by sex, race, and ethnicity.

''(B) The total number of participants who completed the program.

''(C) The indicators required by section 116(b)(2)(A)(i) of the Workforce Innovation and Opportunity Act (29 U.S.C. 3141(b)(2)(A)(i)).

''(2) REPORT TO CONGRESS.—Not later than 180 days of receiving the annual report under paragraph (1), the National Semiconductor Technology Center shall—

''(A) prepare and submit a report containing a summary of the information described in paragraph (1) to the Committee on Commerce, Science, and Transportation and the Committee on Health, Education, Labor, and Pensions of the Senate and the Committee on Science, Space, and Technology and the Committee on Education and Workforce of the House of Representatives; and

''(B) make such report publicly available.

''(h) AUTHORIZATION OF APPROPRIATIONS.—Notwithstanding subsection (d) of section 102 of Public Law 117–167 (commonly known as the 'CHIPS and Science Act of 2022'), amounts made available under subparagraphs (D) and (E) of subsection (d)(2) of such section shall be used to carry out this section for the applicable

fiscal year, and paragraph (3) of section 102(d) of Public Law 117–167 shall not apply.''.

SEC. 6. PROHIBITION ON ADDITIONAL MICROELECTRONICS EDUCATION AND WORKFORCE CLEARINGHOUSE.

A Federal agency shall not establish a microelectronics education and workforce clearinghouse that is duplicative or alternative to the online clearinghouse authorized in section 102(d) of Public Law 117–167 (commonly known as the ''CHIPS and Science Act of 2022'').

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